CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A DC converter, comprising:

a semiconductor switch;

a clock generator for outputting a clock signal to a gate of said semiconductor switch for controlling an on/off time of said semiconductor switch such that a predetermined power is output therefrom; and

a drive circuit for switching said semiconductor switch to a continuous-on state according to a halt mode setting requirement regardless of said clock signal, when said semiconductor switch, normally repeating on/off operations responsive to said clock signal is in an off-state,.

2. The DC converter according to claim 1, wherein said drive circuit comprises a signal synchronization unit for switching said semiconductor switch to a continuous-on state according to said halt mode setting requirement after said semiconductor switch is turned off in response to said clock signal input from said clock generator.

3. The DC converter according to claim 1, wherein said drive circuit comprises an off-signal generator unit for switching said semiconductor switch to a continuous-on state according to said halt mode setting requirement, after said semiconductor switch is forcibly turned off, regardless of said clock signal input from said clock generator.

4. A method for setting up a halt mode for a DC converter, said method comprising the steps of:

receiving a clock signal input at a switch in the DC converter, wherein said clock signal controls an on/off time period for said switch to allow a predetermined amount of power to be output from said DC converter;

determining when said switch is in an off-state; and

receiving a halt mode signal at said switch during said off-state, wherein said halt mode signal turns said switch to a continuous-on state, regardless of the state of said clock signal input.

5. The method according to claim 4, further comprising turning said switch to a continuous-on state in response to said halt mode signal

after said switch is turned off in response to said clock signal input from said clock generator.

6. The method according to claim 4, further comprising switching said semiconductor switch to a continuous-on state in response to said halt mode signal after said switch is forcibly turned off regardless of said clock signal input from said clock generator.

7. A DC converter, comprising:

a semiconductor switch;

a clock generator means for outputting a clock signal to a gate of said semiconductor switch for controlling an on/off time of said semiconductor switch such that a predetermined amount of power is output therefrom; and

a drive circuit means for outputting a halt mode setting requirement, wherein said drive means switches said semiconductor switch to a continuous-on state according to the halt mode setting requirement regardless of said clock signal when said semiconductor switch, normally repeating on/off operations responsive to said clock signal, is in an off-state.

8. The DC converter according to claim 7, wherein said drive circuit means includes signal synchronization means for switching said semiconductor switch to a continuous-on state according to said halt mode setting requirement, after said semiconductor switch is turned off responsive to said clock signal input from said clock generator means.

9. The DC converter according to claim 7, wherein said drive circuit means includes an off-signal generator means for switching said semiconductor switch to a continuous-on state according to said halt mode setting requirement, after said semiconductor switch is forcibly turned off regardless of said clock signal input from said clock generator means.